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SELF-SELECTING PRECHARGED DOMINO LOGIC CIRCUIT

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to domino logic circuits and, more specifically, to such circuits which are selectively precharged.

BRIEF DESCRIPTION OF THE PRIOR ART

Domino logic circuits are well known in the art and generally include in series between a source of power and reference voltage, a first transistor of one of n-channel or p-channel and preferably p-channel, one or more serially connected second transistors of the other of n-channel or p-channel and a third transistor of the same type as the second transistor(s). An output is taken from the node at the junction of the first transistor and second transistor(s) and inverted by an inverter. During the precharge operation, the first transistor is normally conducting and the second and third transistors are normally non-conducting to provide a high signal at the precharge node at the junction of the first transistor and second transistor(s) and a low signal at the inverter output, this being the precharging phase of operation. If the second and third transistors are all then concurrently activated and the first transistor is deactivated, the voltage at the node at the junctions of the first transistor and second transistor(s) will go low

whereas that node will remain high if any of second or third transistors is not activated after precharge. The output of the inverter is the inverse of the voltage at the node. It is therefore apparent that the voltage at the precharge node will not change appreciably if any of the one or more second transistors are not activated in the cycle prior to the next precharge.

Domino logic circuits are generally used in circuitry containing many such circuits, such as, for example, in matrix arrangements or the like wherein only one of plural such logic circuits will be activated at any one time with the other logic circuit being unactivated. It follows that power is wasted whenever a precharge voltage is applied to the precharge node of a logic circuit which has not been activated when the precharge node is already at the high voltage.

SUMMARY OF THE INVENTION

In accordance with the present invention, the above described problem inherent in the prior art domino logic circuits is minimized and there are provided domino logic circuits wherein power is not applied to the precharge node at the junction of the first and second transistors when the voltage at that node is already sufficiently high.

Briefly, the above noted problem is minimized by sensing the status (high or low) at the output of the domino logic circuit and providing a switch in series with the input to the control electrode of the first transistor of the domino logic circuit which is controlled in response to the status of the logic circuit output to isolate the precharging signal from the first transistor when the precharge node is charged to a sufficiently high voltage. In addition, there are optionally provided transistors of the same type as the first transistor, one of which is coupled between a power source and the gate of the first transistor and the other is coupled between a source of power and the precharge node, each of these optional transistors being controlled by the signal at the output node. It can be seen that these optional transistors are activated when the signal at the output node is low to provide a high signal at the gate of the first transistor and at the precharge node. This insures that the first transistor is maintained in the deactivated condition, especially when the gate electrode of the first transistor would otherwise be floating and that the precharge node is maintained with a high signal.

As a further embodiment of the invention, the above described circuit is altered so that the gate of the third transistor is coupled to the gate of the first transistor. In this way, when the first transistor is activated, the third transistor is deactivated and vice versa.

In accordance with a still further embodiment of the invention, the circuit is identical to that of the paragraph immediately above except that the switch is replaced by a CMOS arrangement composed of an n-channel transistor and a p-channel transistor with the n-channel transistor performing the same operation as switch and being connected in the same manner whereas the gate of the p-channel transistor is coupled to the precharge node. Since the signal on the precharge node is high when the signal on the output node is low and vice versa, and since the n-channel transistor forming a part of the switch is rendered conductive by a high signal whereas the p-channel transistor forming the switch is rendered conductive by a low signal, it follows that the addition of the p-channel transistor provides a redundant check on the operation of inverter.

In accordance with a yet further embodiment of the invention, the circuit of the first embodiment is altered by replacing the optional transistor coupled to the precharge node with a feedback inverter which feeds back an inversion of the signal at the output node to the precharge node and by connecting the gate of the third transistor to the PC bar input line coupled to the switch.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a circuit diagram of a domino logic circuit in accordance with the prior art;

FIGURE 2 is a timing diagram for the circuit of FIGURE 1;

FIGURE 3 is a circuit diagram of a domino logic circuit in accordance with a first embodiment of the present invention;

FIGURE 4 is a circuit diagram of a domino logic circuit in accordance with a second embodiment of the present invention;

FIGURE 5 is a circuit diagram of a domino logic circuit in accordance with a third embodiment of the present invention; and

FIGURE 6 is a circuit diagram of a domino logic circuit in accordance with a fourth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGURES 1 and 2, there is shown a typical prior art domino logic circuit 1 having, connected in series between V_{DD} and reference voltage, an n-channel transistor 3 and p-channel transistors 5, 7, 9 and 11. Transistors 5, 7 and 9 are coupled to inputs and, as shown, act as a gate circuit. It should be understood that there can be one or more such transistors 5, 7, 9 with inputs and the fact that the circuit is shown with three such transistors is of no significance. The output of the circuit is provided at the junction of transistors 3 and 5 which is denoted as node A, the signal at node A being inverted by an inverter 13 to provide an inverted output at node B.

In operation, when the PC bar signal goes low, as shown in FIGURE 2, and with one or more of transistors 5, 7, 9 and 11 inactivated, transistor 3 conducts and node A goes high with inverter 13 causing node B to go low. After a short period of time, the PC bar signal goes high and node A remains high. Subsequently, when the PC signal goes high and if the inputs to transistors 5, 7 and 9 are also high at that time, node A will go low and node B will go high. If one or more of transistors 5, 7 and 9 is not activated, node A remains high. It follows that any precharging of node A when one or more of transistors 5, 7 and 9 is not activated is often unnecessary unless the charge at node A has dissipated over time for some reason.

Referring now to FIGURE 3, there is shown a first embodiment of a domino logic circuit in accordance with the present invention

wherein an n-channel transistor 15 is provided in series with the gate or control electrode of transistor 3 of FIGURE 1 and the gate electrode of transistor 15 is coupled to receive the signal which is fed back from node B of FIGURES 1 and 3. In this way, when the circuit is in the precharged state, node A will be high and node B will be low, thereby causing transistor 15 to be inactivated. When node B goes high, transistor 15 is activated and permits the next precharging signal, PC bar, to cause activation of transistor 3 to cause node A to go high. It can be seen that precharging takes place only when necessary, thereby providing a saving of power. In addition, as shown in FIGURE 3, there are optionally provided a p-channel transistor 17 which is coupled between a power source and the gate of transistor 3 and a p-channel transistor 19 which is coupled between a source of power and node A, each of transistors 17 and 19 being controlled by the signal at node B. It can be seen that transistors 17 and 19 are activated when the signal at node B is low to provide a high signal at the gate of transistor 3 and at node A. This insures that transistor 3 is maintained in the deactivated condition, especially when the gate of transistor 3 would otherwise be floating and that node A is maintained with a high signal.

Referring now to FIGURE 4, the circuit is identical to that of FIGURE 3 except that the gate of transistor 11 is coupled to the gate of transistor 3. In this way, when transistor 3 is activated, transistor 11 is deactivated and vice versa.

Referring to FIGURE 5, the circuit is identical to that of FIGURE 4 except that transistor 15 is replaced by a CMOS arrangement composed of n-channel transistor 21 and p-channel transistor 23 with transistor 21 performing the same operation as transistor 15 and being connected in the same manner whereas the gate of transistor 23 is coupled to node A. Since the signal on node A is high when the signal on node B is low and vice versa, and since transistor 21 is rendered conductive by a high signal whereas transistor 23 is rendered conductive by a low signal, it follows that the addition of transistor 23 provides a redundant check on the operation of inverter 13.

Referring now to FIGURE 6, the circuit of FIGURE 3 is altered by replacing transistor 19 with a feedback inverter 25 which feeds back an inversion of the signal at node B to node A and by connecting the gate of transistor 11 to the PC bar line.

Though the invention has been described with respect to specific preferred embodiments thereof, many variations and modifications will immediately become apparent to those skilled in the art. For example, although each of the embodiments of FIGURES 3 to 6 shows only a single n-channel transistor 5 conected between node A and transistor 11, it is understood that one or more additional n-channel transistors could be connected in series with transistor 5 between node A and transistor 11 in a manner similar to transistors 7 and 9 of FIGURE 1. It is therefore the intention that the appended claims be interpreted as broadly as possible in

view of the prior art to include all such variations and modifications.